Claims

What is claimed is:

1. In a multiple plane memory having a common address space and capable of multiple types of memory access operations, each memory plane having independent address decoding logic dedicated to the address space for that plane, a functional register decoding system for routing of command and address information to designated planes, the decoding system comprising:

a plurality of functional registers dedicated to distinct memory access operations, each register configured to receive an input address, and to provide at least one address output in accord with its dedicated memory access operation;

a plurality of plane selector blocks, each plane selector block dedicated to a distinct one of the memory planes, each plane selector block configured to receive as inputs the address outputs from all of the plurality of functional registers, the plane selector blocks routing a selected one of its inputs as an output to its dedicated plane in accord with a control signal input; and

plane function select means configured to receive decoded plane and command information for providing control signals to the plurality of plane selector blocks in accord with the decoded information such that command information for a particular memory access operation and plane information for a particular one of the memory planes are used to route address outputs from the functional register dedicated to that memory access operation to that particular memory plane.

2. A functional register decoding system as in claim 1, wherein the plurality of functional registers include address registers dedicated to any two or more of the memory access operations comprising random access read, burst read, program, erase, and erase-suspend program operations.

3. A functional register decoding system as in claim 2 wherein registers dedicated to burst read and erase operations are counter registers.

4. A functional register decoding system as in claim 2 wherein program and erase operations share a single register dedicated to both types of memory access operation.

5. A functional register decoding system as in claim 1 wherein each register includes a register lock responsive to a lock control signal for selectively enabling or disabling loading of an input address into the register.

6. A functional register decoding system as in claim 1 wherein the plane function select means supports simultaneous operations of different types within different planes, the plane function select means providing control signals to a first plane selector block for routing address outputs from one functional register to a first plane and providing further control signals to a second plane selector block for routing address outputs from a different functional register to a second plane.

7. A functional register decoding system as in claim 1 wherein the plane function select means supports nested operations within a single plane, the plane function select means providing control signals to a plane selector block corresponding to a plane that suspends a first memory access operation in order to carry out a second memory access operation of a different type, then resumes the first memory access operation.

8. A functional register decoding system as in claim 7 wherein the nested operations include an program or erase operation and a read operation.

9. A functional register decoding system as in claim 8 wherein the read operation is a burst read operation.

10. A functional register decoding system as in claim 7 wherein the nested operations include an erase operation and a program operation, the erase and program operations normally sharing a single functional register, the functional registers including a erase-suspend program register for storing an input address corresponding to the nested program operation while the erase operation is suspended.

11. A method of maintaining address information for a plurality of types of memory access operations in a multiple plane memory, each operation destined for execution in a particular one of the memory planes, the method comprising:

(a) receiving address and command information corresponding to a particular memory access operation at an address in a particular memory plane;

(b) storing the address information in a functional register dedicated to the particular memory access operation, the functional register being locked until the operation specified for the address information is completed;

(c) routing the address information from the functional register to the particular memory plane;

(d) repeating steps (a) through (c) for successive received address and command information, except that registers are inaccessible to receiving new address information while locked.

12. A method as in claim 11 wherein the memory access operations having a corresponding dedicated functional register include any two or more of random access read, burst read, program, erase, and suspend-erase program.

13. A method as in claim 11 wherein the repeating step (d) includes simultaneous memory access operations of different types being executed in different memory planes, each operation having address information routed from its corresponding functional register to the memory plane specified for that operation.

14. A method as in claim 11 wherein the repeating step (d) includes nested memory access operations of different types being executed in the same memory plane, the nested memory access operation comprising (1) suspending of a first memory access operation, (2) carrying out of a second memory access operation while the first operation is suspended, and (3) resuming the first memory access operation when the second operation has been completed, each operation having address information routed successively from its corresponding functional register to the specified memory plane, address information in the functional register corresponding to the first memory access operation being maintained while the second operation is carried out so as to be available for when the first operation is subsequently resumed.

15. A method as in claim 14 wherein the nested operations include an program or erase operation and a read operation.

16. A method as in claim 15 wherein the read operation is a burst read operation.

17. A method as in claim 14 wherein the nested operations include an erase operation and a program operation, the erase and program operations normally sharing a single functional register, the functional registers including a erase-suspend program register for storing a address information corresponding to the nested program operation for execution while the erase operation is suspended.